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CMOS-based active RC sinusoidal oscillator with four-phase quadrature outputs and single-resistance-controlled (SRC) tuning laws

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Abstract

This paper proposes a very compact CMOS realization of active RC sinusoidal oscillator capable of generating four quadrature voltage outputs. The oscillator is based on the cascade of lossless and lossy integrators in loop. The governing laws for the condition of oscillation (CO) and the frequency of oscillation (FO) are single-resistance-controlled (SRC) and which allow independent FO tuning. Unlike previously reported SRC-based sinusoidal oscillators based on the active building block (ABB) based approach and which aim at reducing the number of employed ABBs, this direct CMOS realization provides a much reduced transistor count circuit and consequently offers a low power solution. A comparison with previously reported SRC oscillators in terms of number of transistors and current consumption has been provided. As a design example, a 160.2 kHz oscillator (typical process, T = 27°C) with 82 μW power consumption is designed in 65 nm CMOS technology with supply voltage of ±0.5 V.

Keywords: Analog circuits, active RC sinusoidal oscillator, single-resistance-controlled (SRC).

1. Introduction

Sinusoidal oscillators are very important analog circuits and find numerous applications in communication, control systems, signal processing, instrumentation, and measurement systems (see [1] and references cited therein). Active RC sinusoidal oscillators with independent tuning laws for the condition of oscillation (CO) and the frequency of oscillation (FO) are very desirable for independent FO tuning and consequently a lot of research has been done to devise the so called "single-resistance-controlled" oscillators or SRCOs. There have been numerous publications dealing with realizations of SRCOs using variety of active building blocks (ABBs). The recent publications in the field [2]–[15] use wide variety of composite ABBs, each of which is of some type of current conveyor (CC) or its composite (basically employing unity gain voltage followers and current followers) and/or cascade of CC and transconductance amplifier and every work aims to provide a novel implementation for the SRCO with improved features like reduced "ABB count", availability of quadrature outputs, etc.

Many of the recent works are based on "integrator-in-loop" method of designing SRCOs, which has been proposed more than a decade ago and researched well by several authors [16], [17]. Thus, several of the recent works in SRCO design, instead of creating a novel oscillators/ topologies with improved features for integration in mainstream CMOS, rather create a novel ABB and employ the already known SRC design equations (or state variable method, e.g. [16], [17]) to devise the oscillator. Some of the recent works also provide new oscillator topologies to realize different CO and FO tuning laws [18], [19] (including SRC); but there is hardly any explanation on to the use of these novel oscillator topologies over the already established topologies. The authors believe that although the focus of the researchers working in this field since the last several years has been to realize minimum ABB circuit solutions and to demonstrate the concept and/or devise novel topologies, it is also important to use the already established circuit theory in realizing reduced transistor count circuit solutions consuming much lesser power (as compared to ABB based design approach) and thus make the proposed circuit solutions in this field more attractive for mainstream CMOS integration [20]. The authors, of course, do not rule out the advantage(s) of ABB based design approach in creating new circuit solutions and devising additional useful approaches to create the circuit solutions, but believe that having realized a compact ABB based circuit solution, the focus should be on compact CMOS realization of the solution for monolithic integration.

A comparison with recently reported ABB based SRCOs with the proposed CMOS SRCO is provided in Ta-

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Table 1: Comparative study with previously reported SRCOs.

Ref.	ABB type[#]	No. of ABBs	No. of transistors	Frequency of operation (kHz)	Tuning range [max freq → min freq] (kHz)	Amplitude of oscillation mV or μA	THD (%)	Power consumption (mW)
[2]	CCII	2	*D*	–	30 → 9	–	–	–
[3]	FDCCII	1	60	1725	–	V-262	1.4	118.09
[4]	FDCCII	1	60	2240	–	I-70	–	–
[5]	CFOA	2	*D*	15.92	64 → 9	V-8399^{+}	2.47	–
[6]	CFOA	2	*D*	–	–	–	–	–
[7]	CDBA*	2	*D*	974.4	974.4 → 300	V-5400	< 4	–
[8]	CDBA*	2	*D*	15.92	47 → 11	V-8100^{+}	1.58	–
[9]	ICCII$^{\wedge}$	2	18	–	–	–	–	–
[10]	VF/CF**	–	76	950	–	V-350	–	–
[11]	VF / CF**	–	38	930	1600 → 210	V-275	–	–
[12]	DBTA	1	*D*	15.61	46.3 → 10.6	V-7359^{+}	1.63	–
[13]	DBTA	1	*D*	15.88	36.2 → 11.5	V-25.29	2.07	–
[14]	GCFTA / UGVF	2	24	15.92	24.2 → 3.6	V-28 / 29.5$^{\bullet}$	1.67	–
[15]	PCA	3	96	138	296.4 → 46.6	I-1090 / 1240$^{\bullet}$	< 2	24.4
Proposed	–	–	22 / 26	160.2	175.1 → 104.4	V-28	< 2.5	0.082

[#] Refer Appendix for nomenclature of the ABBs
– Not mentioned
* Each CDBA created using two AD844 CFOA ICs, see Fig. 1 [7]
$^{+}$ AD844 IC voltage supply used was $\pm$12 V
$^{\bullet}$ Different amplitudes of quadrature outputs
$^{\wedge}$ Topology 1, circuit 3
D Discrete ICs used
** Uses zero systematic offset voltage follower of Palumbo and Pennisi [25]

ble 1. This list does not include the active-C oscillators that use operational transconductance amplifiers (OTAs) (e.g. circuits in Fig. 2 of [21] and [22]) to actively simulate resistors and are based on the same/similar principle of provide SRC tuning laws as already pointed in [16], [17]. It is clearly evident from Table 1 that the proposed circuit in this paper enjoys low transistor count and low power consumption as compared to many recently reported sinusoidal oscillators based on ABB based design approach. The large power consumption in [3] can be accounted for large tail biasing current used for the differential amplifiers to provide large bandwidth to the ABB and in [15] due to more number of ABBs. Thus, ABB based oscillator designs should focus optimally on both the reduction of ABB count and reduction/optimization of ABB power consumption considering the FO and tuning range of interest to achieve optimal bandwidth and port characteristics of ABB. Power optimization is also true in CMOS oscillator design wherein the biasing current of the transistors needs to be chosen appropriately for the desired operating frequency range and effort should be made to reduce the number of current branches between the supplies. Our design takes cognition of this point. It should also be noted that recently reported CMOS quadrature RC oscillator [23] suitable for RF frequencies is based on the two-integrator in loop method, but it does not provide SRC tuning. Based on the already known technique of creating SRCOs, which is the cascade of lossless and lossy integrator in loop, this paper proposes a reduced transistor count and low power consumption CMOS SRCO. The authors believe that although the underlying principle is already known [16], [17], but the novelty lies in bringing the already known circuit theory (which has been used previously to create ABB based SRCO) to create this CMOS SRCO.

2. Proposed circuit

The proposed CMOS SRCO circuit is shown in Fig. 1. All transistors have source and body tied together to eliminate body effect on threshold voltage. Transistors M_1-M_8 form an integrator, which in the operating frequency range simulates a pseudo lossless integrator: V-I conversion is performed by source degenerated differential amplifier comprising of M_1-M_4, where M_1-M_2 and M_3-M_4 are matched transistors and for high linearity V-I conversion it is required that g_{m1},$g_{m2} \gg 1/R_1$. Without loss of generality, several other high linearity CMOS V-I convertors could be employed, e.g. cross-quad (see Chapter 13 of [24]). Cross coupled transistors M_6-M_7 simulate negative resistance and cancel the positive resistance of the diode connected transistors M_5, M_8. Exactly matched transistors M_5-M_8 provide $2r_{o5}||2r_{o6}||2r_{M1,M2} \approx 2r_{o5}||2r_{o6}$ as the effective output resistance across the terminals $V_{2A}-V_{2B}$, where r_{M1} is the output resistance looking into drains of M_1 and M_2 and $r_{M1} \approx r_{o1}(1 + g_{m1}R_1)$ and which creates a non-zero frequency pole with capacitor C_1, deviating the characteristics as lossless integrator in low frequency range. Transistors M_6-M_7 can be sized slightly larger than M_5, M_8 to provide higher effective output resistance, but this technique should be used with caution as device mismatch can lead to unstable loop if negative resistance is less than positive resistance, i.e. the positive feedback dominates.

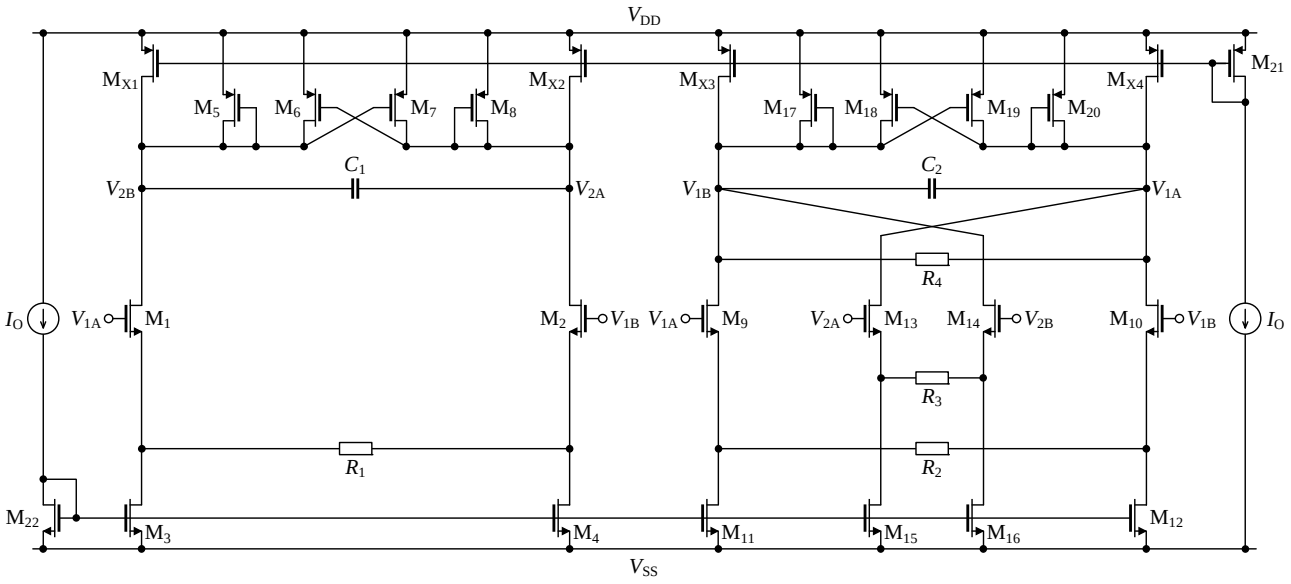

Figure 1: CMOS four-phase quadrature oscillator with SRC tuning law.

Thus, it is required that under all process, voltage, temperature (PVT) conditions $2r_{o5}||2r_{o6}||2r_{M1,M2}||2/(g_{m5}-g_{m6})$ remain positive and which can be ensure through sufficient margin in design.

Additional technique to provide higher output resistance across terminals $V_{2A}-V_{2B}$, to enhance the low frequency output range of the integrator and simulate a lossless integrator, is to reduce the current flowing into M_5-M_8 by using transistors $M_{X1}-M_{X2}$. But note that now the output resistance of M_{X1}, M_{X2} come in parallel to effective output resistance of M_5-M_8 and hence this technique only makes sense if the output resistance of M_{X1} and M_{X2} in the much larger than effective output resistance of M_5-M_8. This can be the case in designs wherein M_5-M_8 cannot be made to maximum length transistors as then they would also have to be large widths so that overdrive voltage of the transistors does not become increasingly large (i.e. to maintain the DC voltages $V_{2A}-V_{2B}$) and this would cause increased parasitic capacitance in parallel to the external capacitor and shift the FO. If $2r_{o5}||2r_{o6}||2r_{ox1}$ is designed to have very large values, the effective output resistance can be limited to $2r_{M1} \approx 2r_{M2} \approx 2r_{o1}(1+g_{m1}R_1) \approx 2g_{m1}r_{o1}R_1$. In any case, the fundamental idea is to provide a high output resistance to effectively simulate lossless integrator within the operating frequency range. Similarly, M_9-M_{12} and $M_{13}-M_{16}$ perform V-I conversion and their currents are subtracted and flown into parallel combination of resistor R_3 and capacitor C_2 to create lossy integrator. M_9-M_{10} and $M_{13}-M_{14}$ are matched transistors of the diff-pair and have same transconductance $g_{m9}=g_{m10}=g_{m13}=g_{m14}$. Also, as before, the requirement $g_{m1} \gg 1/R_1$ needs to be true.

In predicting the condition of oscillation (CO) and the frequency of oscillation (FO), we make some simple assumptions (assumptions should be made true through design), that $g_{m1}r_{o1} \gg 1$, negative resistance-positive resistance cancellation in M_5-M_8 and $M_{17}-M_{20}$ is perfect, all parasitic capacitances (C_{gs}, miller multiplied C_{gd}, etc.) are lumped into external capacitance C_1 and C_2 and $R_2 = R_3$. With these assumptions the simplified CO and FO can be given as:

$$\text{CO}: \quad R_4 \geq \frac{1}{g_{m9}} + R_2, \tag{1}$$

$$\text{FO}: \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2(R_1+1/g_{m1})(R_2+1/g_{m9})}} \approx \approx \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_1R_2}}. \tag{2}$$

It is evident from (1) and (2) that CO can be controlled by R_4 and FO can be controlled by R_1 and thus the proposed oscillator is an SRCO.

The current consumption of the oscillator depends on:

(i) The choice of biasing current to provide transconductance $g_{m1} \gg 1/R_1$ and $g_{m9} \gg 1/R_2$. This condition is required so that FO primarily depends on the resistance value and hence be well controlled with temperature variations unless the current bias is derived from a constant-g_m circuit such that the inverse of transconductance is servo to scaled value of a low-tempco resistor in the current generation circuit. Considering the main transistors of the diff-pairs M_1-M_2, $M_{13}-M_{14}$, and M_9-M_{10} are biased in sub-threshold region to provide large transconductance for a given bias current, we get $I_{DM1}=I_{DM2} \gg nV_T/R_1$ and $I_{DM9}=I_{DM10}=I_{DM13}=I_{DM14} \gg nV_T/R_2$.

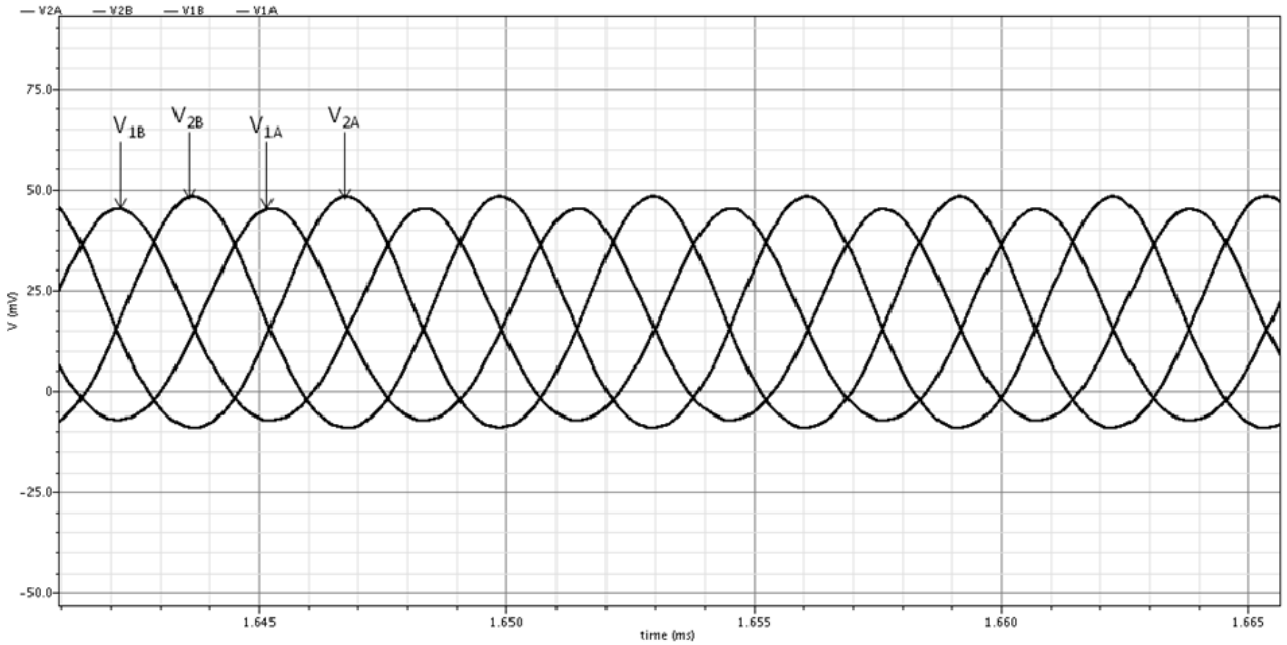

Figure 2: Oscillation waveforms for the four-phase quadrature oscillator.

(ii) Increase in tail current to increase the transconductance g_{m1} would also require a proportional increase in the bias currents of $M_{X1}-M_{X2}$. Similar increase is also required for the bias currents of $M_{X3}-M_{X4}$. This design chooses $I_{DMX1} = I_{DMX2} = I_{DMX3} = I_{DMX4} = 0.8\ I_{DM3}$.

(iii) Also, to ensure the same DC bias point at V_{1A}, V_{1B}, V_{2A}, V_{2B} it is required that $I_{DM11} = I_{DM12} = I_{DM13} = I_{DM14} = 0.5\ I_{DM3} = 0.5\ I_{DM4}$.

Table 2: Aspect ratio of the transistors.

Transistors	W/L (μm/μm)
M_9, M_{10}, M_{13}, M_{14}	10*10/0.3
M_1, M_2	10*20/0.3
M_5, M_8, M_{17}, M_{20}	6/1
M_6, M_7, M_{18}, M_{19}	6.4/1
M_{11}, M_{12}, M_{15}, M_{16}	3*10/5
M_3, M_4	3*20/5
M_{20}, M_{21}	5/5
$M_{X1}-M_{X4}$	5*16/5

3. Design strategy and simulation results

The circuit in Fig. 1 is designed in 65 nm CMOS technology with ±0.5 V supply and with typical NMOS V_{TH} = 450 mV and PMOS V_{TH} = 400 mV. The aspect ratios of the transistors in Fig. 1 are given in Table. 2. All the transistors are biased well into saturation except the main transistors of the diff-pairs M_1-M_2, $M_{13}-M_{14}$, and M_9-M_{10} which are biased in sub-threshold region to provide large transconductance. Moreover, biasing these transistors in sub-threshold make their V_{GS} much less than V_{TH} (by about 100 mV) and which helps keep the tail currents of the diff-pair well into saturation.

Current mirror transistors at the tail of the differential amplifiers M_3-M_4, $M_{11}-M_{12}$, $M_{15}-M_{16}$ are designed with maximum length (5 μm) to provide high output resistance, provide better current mirroring and reduce random mismatch between transistors, which reduces with increased area. With increased length, the widths also have to be correspondingly increased so that over-drive voltages are not increased too much and maintain all transistors in saturation. Note the choice of maximum length transistors for current mirrors is just an example and reduced length and width transistors (e.g., both scaled down by factor of 2) can also be used for tail current biasing.

The choice of passive components is important from both circuit functionality and area. It is desirable to keep reduced capacitor size as in current CMOS technologies capacitance/unit area for linear metal-insulator-metal (MIM) capacitors is not very large (≈ 2–3 [fF/μm^2]). However, the minimum capacitor size is limited not only by mismatch, but also transistor parasitic start to play dominant role if the external capacitor is small and hence, FO is not well controlled. Not keeping very small valued capacitors, i.e. using large valued capacitors, is also beneficial for simulating pseudo-lossless integrator (with fixed biasing current) in the operating frequency range as the pole frequency ($1/r_o||C$) is pushed to lower frequencies, leading to better realization of lossless integrator.

For the passives p+ poly-silicon resistors and MIM capacitors (2.5 fF/μm^2) are employed. The values of the passive elements were chosen as: $R_1 = R_2 = R_3 = 50$ kΩ, $R_4 = 58$ kΩ, and $C_1 = C_2 = 20$ pF (Table. 3). The bias current is equal to $I_o = 1$ μA and the entire circuit consumes 82 μA of current. Thus, the power consumption of

Table 3: Component values for FO = 160.2 kHz.

R_1, R_2, R_3	50 kΩ
R_4	58 kΩ
C_1, C_2	20 pF
I_o	1 μA
Total current consumption	82 μA

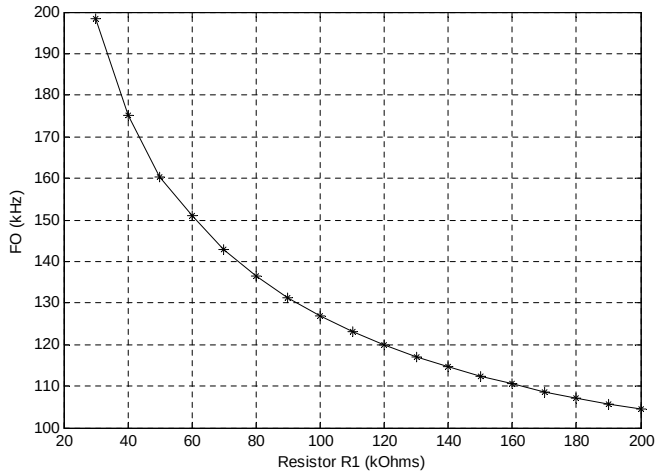

Figure 3: SRC tuning of FO via R_1.

the circuit is 82 μW and which is much lower than many recently reported sinusoidal oscillators based on ABB-based approach [2]–[15]. Note that R_4 value has been chosen to satisfy CO and in the present design, $g_{m9} \approx 250$ μA/V. In industrial designs sufficient margin needs to be given for oscillator start-up across different process and temperature corners. Since g_m varies with temperature, for designs where R_2 is not much larger than $1/g_{m9}$, a constant-g_m bias circuit may to be employed [20] for biasing the tail current of the differential amplifier, to servo the inverse of transconductance value to a low temp-co resistor. The biasing circuit is not shown here and simulations are performed only at typical process and T = 27°C for demonstration of concept. Also, note that increased value of R_4 provides higher oscillation amplitude, but with correspondingly higher distortion. High amplitude oscillations may be useful in some applications, where low THD sinusoids are not required, but rather increased amplitude sine like waves are used to generate square wave using a comparator. In the present design, automatic gain control (AGC) loop has not been employed to control the oscillation amplitude, but it can be done routinely by employing a peak amplitude detector and controlling the bias current of the differential amplifier in negative feedback.

The oscillation waveforms for the four-phase quadrature outputs with FO = 160.2 kHz, where the phase error is less than 1.5° are shown in Fig. 2. The harmonic distortion at each output is less than 2.5% and which can be high in some applications. As described before, an auxiliary AGC circuit is required to regulate the amplitude and improve THD performance. To further demonstrate tuning of FO by simply changing R_1 value, R_1 is varied from 30 kΩ to 200 kΩ and the FO varies from 198.5 kHz to 104.4 kHz, see Fig. 3. In IC design, value of R_1 can be changed in analog fashion by making R_1 as a series combination of fixed linear resistor and triode biased MOSFET. Digital tuning can be achieved by switching unit resistors or binary weighted resistor bank by an external digital code.

Another aspect which needs to be addressed is the usability of the present oscillator as a single frequency generator. On-chip RC oscillators suffer from process variations of both the resistor and capacitor and thus the oscillation frequency tends to vary by as much as ±30% (example, an oscillator designed for 30MHz typical FO can vary from 20MHz to 40MHz). Therefore, on-chip single frequency generators should have mechanisms to be tuned to the appropriate frequency. Most of the on-chip RC oscillators employ a frequency locked loop (FLL) for process compensation wherein the RC oscillator frequency is locked to an external frequency reference (derived from crystal oscillator) or it is multiple. The aim of this work is not the design of an FLL for process compensation, which is a standard technique of frequency locking, but rather to demonstrate the usability of the proposed oscillator to also be embedded in an FLL. As demonstrated, the FO of the proposed oscillator can be varied independently using resistor R1 and thus if embedded in a negative feedback loop the value of the R_1 can be adjusted so that error between the generated output frequency and the reference frequency tends to zero. As already pointed out, R_1 can be changed in analog fashion by making R_1 as a series combination of fixed linear resistor and triode biased MOSFET and also through a digital code by switching unit resistors in series or parallel combination to create the effective R_1. In the analog FLL, the negative feedback loop always needs to be there, necessitating a dedicated input reference frequency, but slow environment changes (e.g. temperature changes) can be tracked and compensated for by the feedback. This also means that the analog FLL will always consume power in the feedback elements that are always ON. In cases where in the user cannot provide a dedicated clock source for continuous time monitoring of the FO but only for one time process trimming, a digital FLL is a better solution. Digital FLL would first of all require the sine wave to be created into square wave for frequency comparison with the input clock. Digital FLL would use a digital frequency detector, which would count the number of cycles of the generated RC oscillator frequency in a reference time period created by the input reference clock. Depending on the count and comparing it with the ideal count, an error count can be generated and through which unit resistors in the R_1 resistor ladder can be switched. Once the RC oscillator frequency is within the desired error bound decided by the resolution of the resistor ladder digital-to-analog converter, the negative feedback loop is disabled, the input reference frequency can be removed and the complete digital frequency detector can be power-down. Further environment changes can never be tracked

out as the oscillator now is free running and can only lead to errors in the FO. Further to be noted is that both the digital and analog loops can have smaller input reference frequency than the RC oscillator frequency and the desired scaling factor can be incorporated within the loop gain. In cases where external frequency reference is not available, off-chip precision passive components are required to set the FO. Servo biasing feedback loops can also be employed to servo on-chip component values to scaled value of the off-chip passive components.

4. Concluding remarks

A compact CMOS realization of active RC sinusoidal oscillator capable of generating four quadrature voltage outputs has been proposed. Based on the concept of cascade of lossless and lossy integrators in loop, the oscillator circuit provides SRC type tuning laws and attempts to reduce the transistor count as opposed to previous approaches of reducing ABB count. It is expected that the circuit is of practical use to researchers and engineers in the field and further advances in creating CMOS RC oscillators with improved features and/or new techniques are reported in the near future.

5. Appendix

This section provides full nomenclature of the aforementioned ABBs.

CCII:	Second-generation current conveyor
CDBA:	Current-differencing buffered amplifier
CF:	Unity gain current follower
DBTA:	Differential-input buffered and transconductance amplifier
FDCCII:	Fully-differential second-generation current conveyor
GCFTA:	Generalised current follower transconductance amplifier
ICCII:	Inverting second-generation current conveyor
PCA:	Programmable current amplifier
UGVF:	Unity-gain voltage-follower
VF:	Unity gain voltage follower

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